PDB BMS Test Cable

Model Number: THRSLTCA1071

Overview

Interface harness between the **PDB** and the **BMS card** for power, serial communications, display, and relay control. The loom brings out service tails for 24 V/12 V inputs and a 24 V output, with shielded signal pairs for noise immunity. Proven in the **UXOR project supplied to the IAF**.

Technical Specifications

Parameter	Specification
Function	PDB ↔ BMS card comms, display power, relay control, and power I/O
Primary connector	**C5:** 62IN-12E-14-19S (to PDB)
Other terminations	BMS card headers (X3/ISP), service tails for **24V-IN1**, **12V-IN2**, **24V-OUT**, and GND
Supported signals	RS-232 (two ports), +5 V, +12 V, +24 V, GND, relay control lines
Cable construction	Shielded/PTFE signal pairs; 20 AWG power conductors; strain-relieved transitions
Environmental	IP65; −20 °C to +55 °C

Pin Configuration (Start → End mapping)

A) To Main Controller (Serial-0)

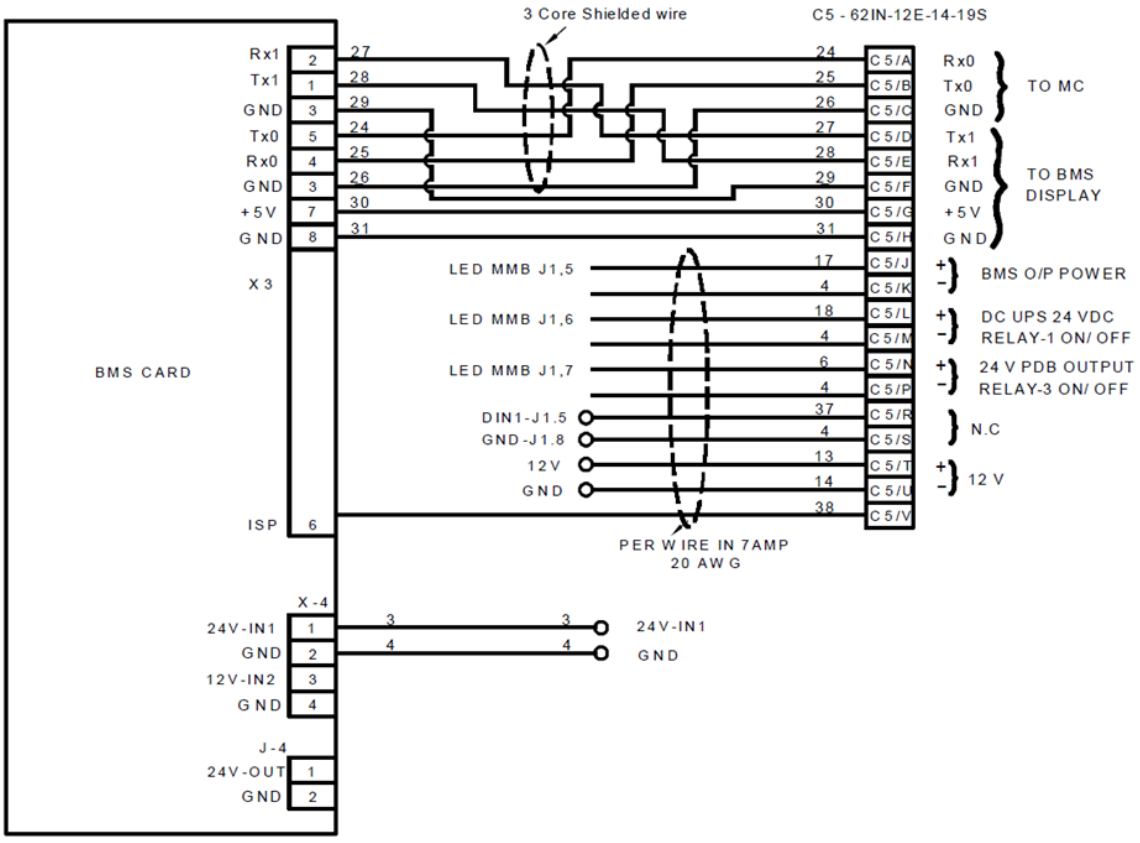
PDB C5 pin	Signal	Destination
A	RX0	MC serial-0 RX
B	TX0	MC serial-0 TX
C	GND	MC signal ground

B) To BMS Display (Serial-1 & +5 V)

PDB C5 pin	Signal	Destination
D	TX1	BMS display TX
E	RX1	BMS display RX
F	GND	Display GND
G	+5 V	Display supply
H	GND	Return

C) BMS Outputs / Relays / Aux

PDB C5 pin	Function	Notes
J	BMS O/P POWER	Status/LED drive (J1.5 → pin 17 on BMS card)
K	DC-UPS 24 VDC RELAY-1 ON/OFF	Control line
L	LED MMB (J1.7)	Status output (per drawing)
M	24 V PDB OUTPUT RELAY-3 ON/OFF	Control line
N	GND (J1.8)	Common return
R	N.C.	Not connected
T	+12 V	Aux supply to BMS card
V	GND	Power return
Body	Shield	Chassis/overall braid continuity



Key Features

- Consolidates **MC comms, BMS display power, relay controls, and power I/O** in one harness.
- Shielded serial pairs and common ground strategy minimize noise.
- Clear labeling for quick commissioning.
- Rugged MIL circular at the PDB side; strain-relieved branch transitions.

Applications

- PDB–BMS integration on UXOR platforms.
- Bench bring-up and EOL testing.
- Field diagnostics where fast swap/trace is needed.

Note

If you want a one-page **wiring aide** for the test bench, I can generate a minimal “PDB C5 → destination” card from this table for lamination.